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Pulsed Transfer Etching of PS–PDMS Block Copolymers Self-Assembled in 193 nm Lithography Stacks

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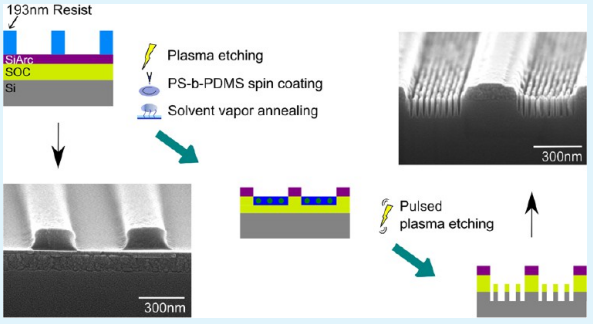
ABSTRACT: This work presents the graphoepitaxy of high-χ block copolymers (BCP) in standard industry-like lithography stacks and their transfer into the silicon substrate The process includes conventional 193 nm photolithography, directed self-assembly of polystyrene-block-polydimethylsiloxane (PS-*b*-PDMS) and pulsed plasma etching to transfer the obtained features into the substrate. PS-*b*-PDMS has a high Flory–Huggins interaction parameter (high-χ) and is capable of achieving sub-10 nm feature sizes. The photolithography stack is fabricated on 300 mm diameter silicon wafers and is composed of three layers: spin-on-carbon (SoC), silicon-containing anti-reflective coating (SiARC) and 193 nm photolithography resist. Sixty-nanometer-deep trenches are first patterned by plasma etching in the SiARC/SoC stack using the resist mask. The PS-*b*-PDMS is then spread on the substrate surface. Directed self-assembly (DSA) of the BCP is induced by a solvent vapor annealing process and PDMS cylinders parallel to the substrate surface are obtained. The surface chemistry based on SoC permits an efficient etching process into the underlying silicon substrate. The etching process is performed under dedicated pulsed plasma etching conditions. Fifteen nanometer half-pitch dense line/space features are obtained with a height up to 90 nm.



KEYWORDS: *directed self-assembly (DSA), PS-b-PDMS, graphoepitaxy, plasma etching, silicon nanostructures*

I. INTRODUCTION

Because of the increased capabilities of electronic devices and their decreasing critical dimensions, the demand for nanoscale fabrication methods has expanded in recent years. As alternatives to standard UV projection photolithography, sophisticated top-down approaches like e-beam,[1] EUV or X-ray[2] lithography have shown promising results in terms of improved resolution but at high cost and or low throughput. In parallel, more cost-effective high-resolution fabrication methods have been developed like nanoimprint lithography[3,4] or block copolymer (BCP) self-assembly.[5] The combination of this latter bottom-up approach with a cost-effective top-down technique is a productive way to obtain high resolution features at a reasonable cost.[6] Indeed, directed self-assembly (DSA) of BCP produces thin films with various nanosized patterns[6−10] and feature sizes smaller than 10 nm.[10−12] It was consequently introduced in the International Technology Roadmap for Semiconductors (ITRS) in order to complement advanced optical lithography techniques by increasing the resolution.[13] In this work, we present the self-assembly of high-χ block copolymers as a complement to conventional 193 nm wavelength photolithography.

BCP consist of two (or more) immiscible polymers that are covalently bonded and undergo a phase separation when enough energy for block movement is provided. Different morphologies (spheres, cylinders, lamellae) are then obtained, mainly depending on the volume fraction of each phase.[14] On planar substrates, self-assembled features are aligned in small areas not larger than a few micrometers but when deposited on topographically modified surfaces (graphoepitaxy process) lithographed patterns can guide the BCP self-assembly over long-range orders.

The Flory–Huggins parameter χ reflects the incompatibility between the two blocks of a copolymer. The higher the χ-value, the higher the achievable pattern resolution. Nowadays, most of the research on BCP lithography is concentrated on polystyrene-block-poly(methyl methacrylate) (PS-*b*-PMMA) because of its ease of processing. This copolymer is commercially available and can be processed quite easily by thermal annealing and integrated with existing microelectronic tools.[12] Nevertheless, PS-*b*-PMMA has a low Flory–Huggins parameter χ (χ = 0.06 at 298 K[15]), limiting its resolution. For this reason, high-χ BCPs like PS-*block*-polyethylene (PS-*b*-PEO), polydimethylsiloxane-block-poly-2-vinylpyridine

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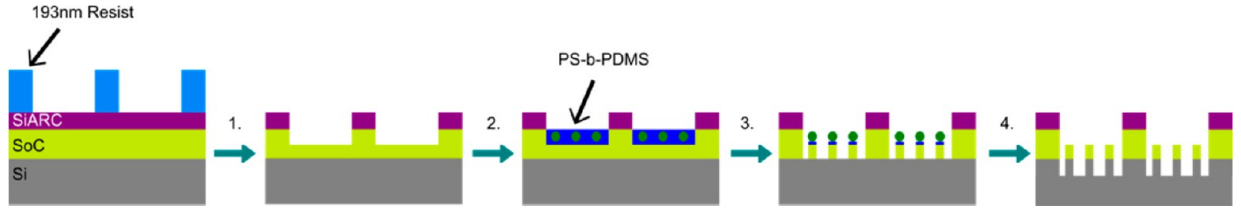

Figure 1. Schematic of the integration process of PS-*b*-PDMS with a standard trilayer 193 nm photolithography stack: (1) Plasma etching in the SiARC and SoC layers using the 193 nm photolithography resist mask; (2) PS-*b*-PDMS spin coating, self-assembly by SVA, and short plasma etching to reveal the oxidized PDMS nanostructures; (3) transfer etching into the remaining SoC layer and (4) into the underlying silicon substrate.

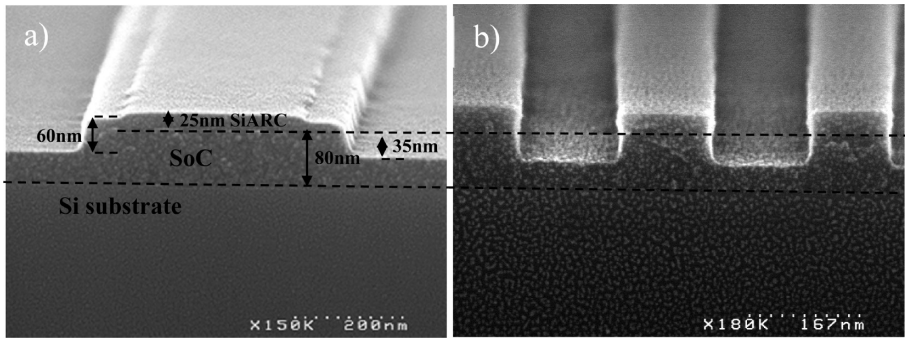

Figure 2. Cross-section SEM images of the SiARC/SoC graphoepitaxy template. (a) 500 nm and (b) 100 nm large lines.

(PDMS-*b*-P2VP), polystyrene-block-poly(styrene-*b*-lactide) (PS-*b*-PLA) or polystyrene-block-polydimethylsiloxane (PS-*b*-PDMS) are gaining more interest.[12] PS-*b*-PDMS shows in particular several advantages.[7,11,16,17] Its χ value is 0.26 at 300 K.[15] This allows smaller periodicities and/or sharper interfaces (periodicity of ∼10 nm). Furthermore, the PDMS block contains a high quantity of silicon, which generates a good etching contrast with the PS block and makes it a robust hard mask for further lithography processes.[17] More precisely, the PDMS block easily forms silicon oxide structures under oxygen plasma, whereas the PS block is degraded under the same treatment.[18,19]

However, because of the high incompatibility of the two blocks, thermal diffusion is not effective enough to thermally produce self-assembly in reasonable processing times. Hence, other nonstandard self-assembly methods have to be introduced.[20] The most common method is solvent vapor annealing (SVA) where the sample is exposed to a solvent vapor. Solvent molecules swell the BCP thin film, reducing the diffusive energy barrier and allowing the self-assembly to take place at room temperature.[16]

In this work, a complete process of directed self-assembly of PS−PDMS in standard spin-on-carbon (SoC)/silicon-containing anti-reflective coating (SiARC) layers and their transfer into silicon by pulsed plasma etching is developed. In the following sections, the technological steps are detailed.

In Figure 1, a schematic of the process flow is presented. First, the photolithography mask is used to etch the SiARC layer and partially the SoC layer to create the self-assembly template (step 1). Then, the cylinder forming PS-*b*-PDMS film is deposited in the trenches and self-assembled by solvent vapor annealing (step 2). Self-assembled structures are transferred into the remaining SoC layer in step 3 and finally into the silicon substrate by dedicated pulsed plasma etching processes (step 4).

2. DIRECTED SELF-ASSEMBLY OF PS-*B*-PDMS

2.1. Plasma Etching Reactor. Experiments are performed in a 300 mm diameter AdvantEdge ICP (inductively coupled plasma) etch tool from Applied Materials as described in.[21,22] The plasma is excited inductively by a Radio Frequency (RF) power source at 13.56 MHz via two concentric RF coils (ICP coil) in order to produce a uniform ions flux. The wafer is biased independently using a second power supply capacitively coupled to the electrostatic chuck. Two modes are available in the etching tool: a continuous wave (CW) mode where the plasma is excited with constant RF power and a "pulsed" mode, in which the ICP source and the bias power supply are pulsed synchronously (via a Pulsync Applied Materials RF system). Typical pulsing frequencies are between 100 Hz and 20 kHz, with duty cycles between 10 and 90%.[23,24] In this work, both CW and pulsed mode are used depending on the etching step.

2.2. Etching Process for Template Preparation. The graphoepitaxy of horizontally oriented PDMS cylinders on topographically modified substrates allows the production of long-range order aligned nanostructures. The prepatterned substrate, consisting of the described SiARC/SoC layers, is obtained with plasma etching in CW mode using a conventional 193 nm wavelength photolithography mask. This mask was generated with last generation resists on 300 mm wafers, using a SOKUDO RF3 coating track interfaced with a Nikon S307E 0.85NA dry ArF scanner. All parameters used were set based on suppliers recommendations. Achieved resolution is better than 100 nm. $Ar/CF_4/CHF_3$ and HBr/O_2 chemistries are used for SiARC and partial SoC etching, respectively. Scanning Electron Microscopy (SEM) cross-section images of obtained trenches (widths varying from 100 to 500 nm) are shown in Figure 2. The trenches consist of an approximately 25 nm thick SiARC and 35 nm thick SoC layer, leading to a total trench depth of about 60 nm. The process conditions are adjusted so that at the end of the process, no photoresist remains on the SiARC layer. However, this complete lift off of the photoresist is at the expense of layer uniformity on the

larger lines (Figure 2, left) because no etch-stop barrier layer is provided. Nevertheless, the nonuniformity of the SiARC layer was found not to be critical in the graphoepitaxy process.

2.3. PDMS Horizontal Cylinders Formation. Diblock copolymer of cylinder forming PS-*b*-PDMS ($M_{PS\text{-}b\text{-}PDMS}$ = 45.5 kg mol^{-1} in which M_{PDMS} = 14.5 kg mol^{-1}), was purchased from Polymer Source, Inc. Toluene and propylene glycol monomethyl ether acetate (PGMEA) were used as solvents.

The PS-*b*-PDMS is dissolved in PGMEA (1, 1.5, and 2 wt %) and spin-coated (1000−3000 rpm) onto patterned SiARC/SoC templates. PGMEA is a common lithography solvent that provides a better wetting of the SiARC/SoC sample surfaces compared to spin-cast solutions prepared with toluene. Self-assembly is performed by solvent vapor annealing in a closed vessel with saturated toluene vapor at room temperature and atmospheric pressure for 3 h. Then, samples are taken out and exposed to dry air to evaporate the solvent. Conditions (BCP dilution, spin speed and trenches opening ratio) were adjusted to yield a polymer thickness of 30 nm into the trenches after SVA. This thickness is close to the natural self-organization period (L_0) of the used polymer ($L_0 \approx 35$ nm).

To efficiently direct the alignment and facilitate the long-range ordering of horizontal cylinders along patterned trenches, both the sidewalls and the bottom of the trenches should present a preferential attraction to the major block of the copolymer. Modifying the surface chemistry of the substrate is known to have strong effects on the orientation of the PDMS cylinders.[25] Therefore, scanning transmission electron microscopy (STEM) imagery was performed on self-assembled PS−PDMS within SiARC/SoC trenches (Figure 3) to evaluate the wetting behavior of PS-*b*-PDMS. The PDMS cylinders that can be seen in Figure 3 show an elongated form. This has already been observed elsewhere[26] and is due to the solvent evaporation during SVA when going from the swollen to the final dried state.[20] Significant strain is induced on the film during drying which can affect the dimension and shape of the nanostructures.

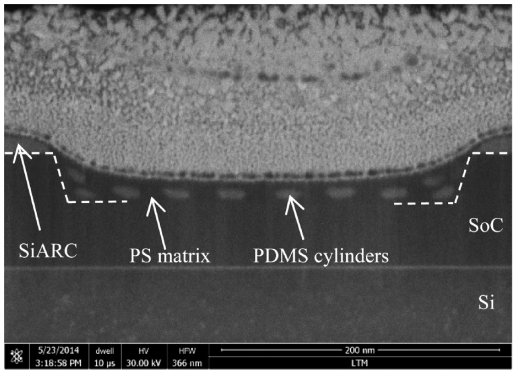

Figure 3. Dark-field STEM images of PDMS cylinders in the PS-matrix formed after SVA in SiARC/SoC trenches.

Due to the high chemical similarity between SoC (mostly composed of carbon) and PS, no PDMS wetting layer between the copolymer and the bottom of the trenches is found. This observation can further be confirmed by the fact that the transfer etching of the PDMS lines into the SoC layer can be carried out with a simple HBr/O_2 plasma (see section 3.1). A PDMS wetting layer at the interface would be oxygen resistant, and would consequently not allow such a transfer etching. This wetting behavior allows indeed the wetting of the PS block (BCP matrix) and thus in addition the rapid formation of horizontal PDMS cylinders parallel to the trenches.

Additionally, a top PDMS wetting layer is present at the BCP surface because of its lower surface energy compared to PS. In Figure 3, this layer is not clearly evidenced, most likely because of a poor contrast between this Si-containing layer and the metallization layer.

Water contact angle measurements on PS-brush, PDMS-brush, and the BCP are emphasized though the presence of a PDMS surface layer. The water contact angles of PDMS- and PS-brush have been reported to be approximately 114 and 95° respectively. The as-spun BCP film and solvent vapor annealed film on planar SoC substrates were found to have a water contact angle of about 109 and 108°, respectively, indicating PDMS rich surface layers. Furthermore, it has been found that plasma etching requires a short CF_4 burst (withdrawal of the PDMS surface layer) to efficiently reveal and transfer the assembled PDMS lines.

Examples of SEM cross-section and top-view of aligned horizontal PDMS cylinders within SiARC/SoC trenches are reported in Figure 4. Here, to visualize the pattern, short CF_4 and HBr/O_2 plasma processes are used respectively to remove the PDMS surface layer and partially etch the PS matrix (The roughness observed between the PDMS lines is due to PS residues not yet completely etched during this transient state).

3. DRY ETCHING PROCESS OF THE DSA-BCP/SOC/SI STACK

Transferring the dense array of lines produced by DSA into the underlying substrate is particularly challenging with common plasma processes, due to the inherently high aspect ratio of the

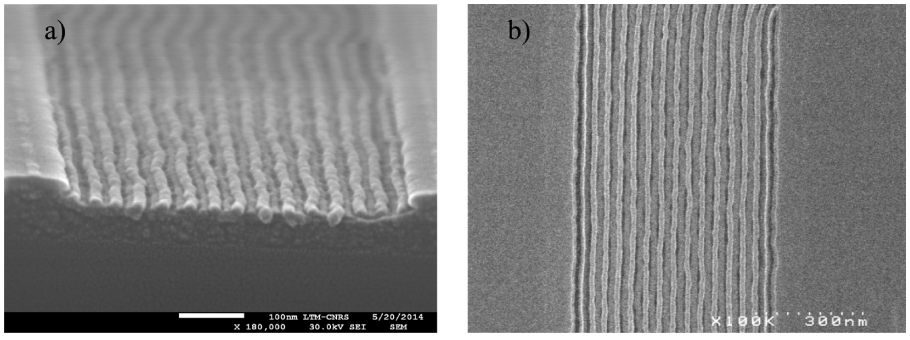

Figure 4. (a) Cross-section and (b) top-view SEM images of directed self-assembled horizontal PDMS cylinders in the SiARC/SoC topographical template after 5 s CF_4 and 5 s HBr/O_2 plasma treatments.

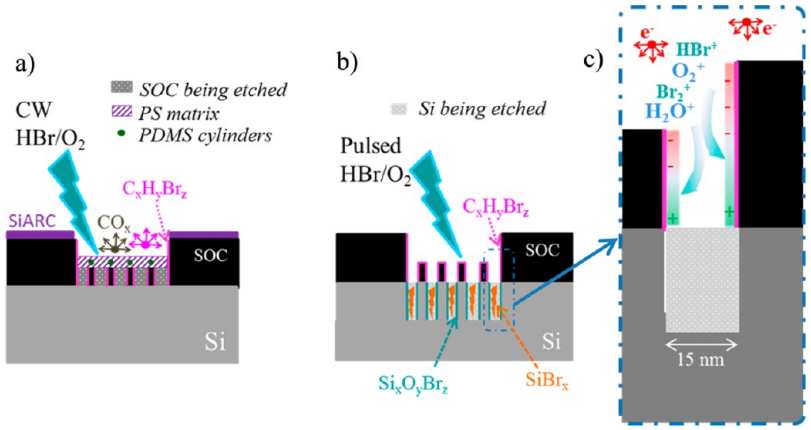

Figure 5. Schematic of the dry etching method used for the PS–PDMS/SoC/Si stack plasma processing. (a) CW HBr/O_2 plasma treatment to eliminate the PS matrix and transfer the pattern into the SoC layer, (b) Si transfer by pulsed HBr/O_2 plasma etching, (c) details of the induced charge distribution during step b.

15 nm lines. The stack is composed of a thin PDMS layer formed at the air/BCP interface, horizontal PDMS cylinders in a PS matrix, a SoC layer and the silicon substrate. Three etching steps are required for transferring the PDMS patterns into the silicon substrate: one to remove the PDMS layer at the top surface, a second one to etch at the same time the unprotected PS-matrix and the SoC layer and a third one to reproduce the pattern into the silicon substrate. Figure 5 illustrates these two last steps and the main chemical species involved.

3.1. Lithographic Mask Formation. Both the revelation (top PDMS wetting layer and PS matrix removal) and transfer of the PDMS lithographic mask in the SoC layer are realized in CW mode (step A and B in Table 1). First, the PDMS wetting layer at the air/BCP interface is removed by a 5 s CF_4 plasma (Step A). Then, the PS matrix of the BCP and the SoC layer are etched using a 25 s HBr/O_2 plasma (Step B). PS and SoC, being essentially composed of carbon, are removed with higher selectivity during this process step compared to PDMS. Indeed, oxygen radicals react with the carbon of the PS/SoC layer to form CO_x volatile etch products. Furthermore, the introduction of bromine leads to the formation of weakly volatile etch products such as $C_xH_yBr_z$ which can redeposit on the feature sidewalls and form a thin protection layer (pink walls on the schematic in Figure 5a). This passivation layer protects the sidewalls from lateral etching, allowing an excellent anisotropic etch of the lines. At the same time, the PDMS cylinders are oxidized and transformed into a SiO_2-like material. Examples of samples obtained after this etching step are reported in Figure 6. High-aspect-ratio lines with vertical sidewalls are obtained.

Table 1. Details of the Etching Process for PDMS Pattern Transfer

step[a]	etching mode	pressure (mTorr)	gas	time (s)	bias power (W)	source power (W)
A	CW	4	CF_4 100 sccm	5	20	700
B	CW	5	HBr/O_2 70/30 sccm	5–25	120	500
C	Pulsed (*Duty cycle =20%*)	20	HBr/O_2 200/5 sccm	10–250	100	750

[a]Step A, PDMS wetting layer removal; step B, PS matrix and SoC layer etching; step C, transfer of the PDMS pattern into the silicon substrate.

3.2. Transfer Etching into the Silicon Substrate. The difficulty of etching high-aspect-ratio features lies in particular in the collection angle of the plasma neutrals (as seen from the trench bottom or sidewalls). The angle is restricted by shadowing the adjacent features, thus decreasing the passivation layer thickness on the sidewalls when increasing the aspect ratio. The lateral etching of features may then become important leading to a lift-off effect of the mask. Furthermore, insulating materials such as oxidized PDMS (and probably passivated SoC) are known to accumulate electric charges. As a consequence, the top of the feature sidewalls is negatively charged, and their bottom positively because the positive ions are directional, whereas the plasma electrons have an isotropic velocity distribution function.[27] As a result, the ions are slowed down and deviated toward the sidewalls. Figure 5c schematizes these phenomena. Consequently, at the bottom of a high-aspect-ratio feature, the ion flux and energy is much lower than on planar substrates and etching can then stop or become too slow to ensure a reasonable etching depth with the available mask thickness. To overcome those issues, one possibility is to use pulsed plasmas. First, pulsing the plasma allows a precise control of the plasma chemistry,[28] and second, pulsed plasma tends to reduce or even eliminate charging of the features.[29] It also helps to overcome any charging by providing extremely energetic ions to the wafer compared to typical CW processes.[24]

In the pulsed plasma system used, the RF power delivered to the ICP coils is modulated ON and OFF periodically at 1 kHz (pulsing period of 1 ms) with a duty cycle of 20% (percentage of RF ON time). All the other parameters (gas flow, temperature, pressure, etc.) are kept constant with a baseline process composed of HBr/O_2 plasma with a low amount of oxygen (Table 1-Step C).

Figure 7 shows the etching profiles obtained after different plasma etching times. The 120 s process allows etching of about 43 nm deep silicon lines, whereas a 200 s process allows patterning 90 nm deep silicon lines. The averaged silicon etching rate is found to be ~0.4 nm/s with a Si/SoC etching selectivity of about 2.5 indicating that the mask is partially consumed during the process. Thus, a thick layer of SoC is necessary to maintain the pattern profile. ;. However, the SoC

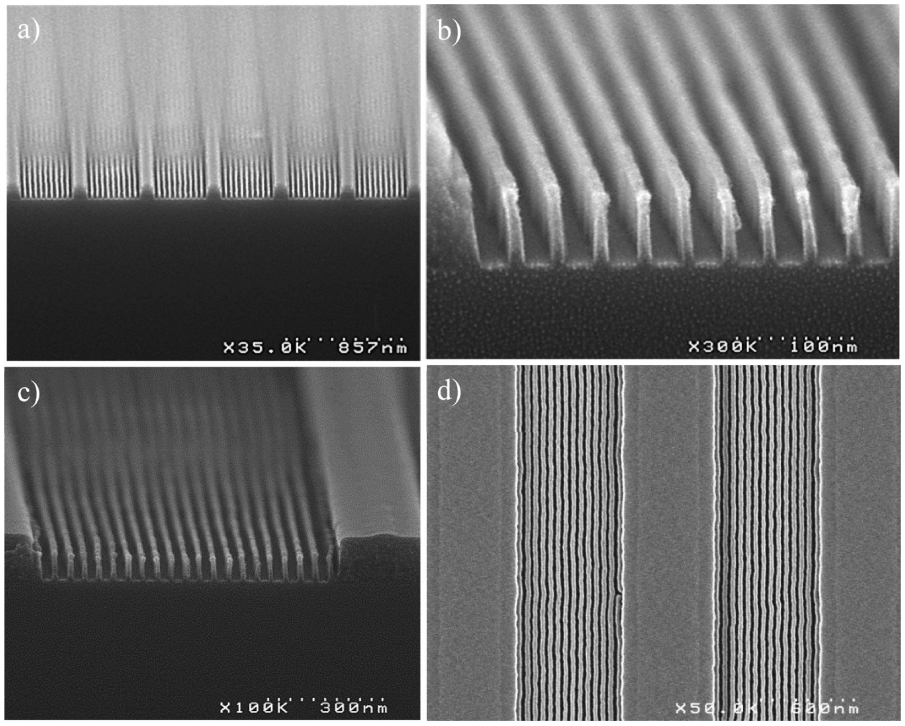

Figure 6. (a–c) Cross-section and (d) top-view SEM images of directed self-assembled horizontal PDMS cylinders transferred into a SoC layer after 5 s CF4 and 25 s HBr/O_2 plasma treatments.

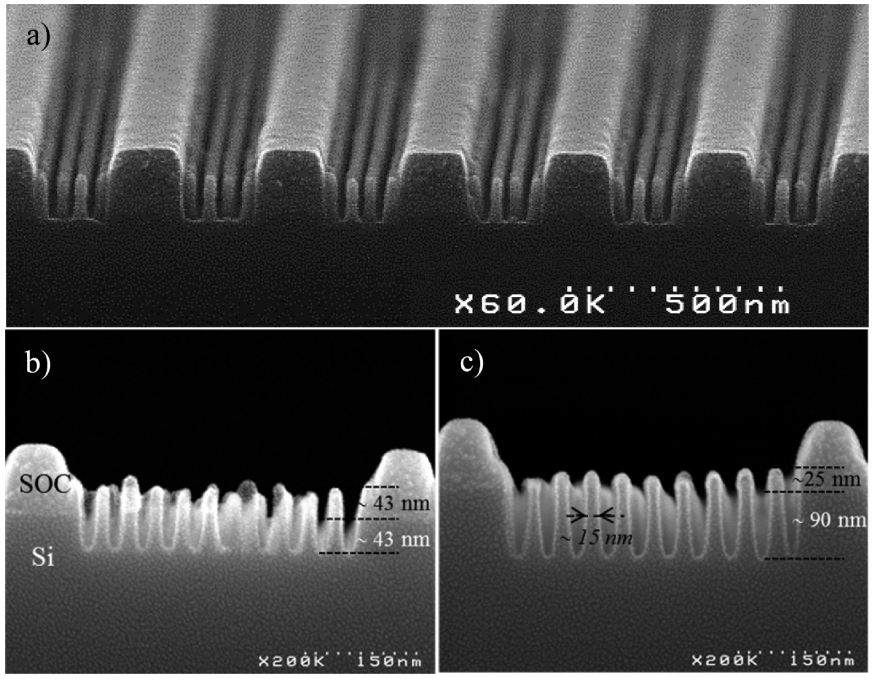

Figure 7. Cross-section SEM images of the transfer etching in the silicon substrate of directed self-assembled horizontal PDMS cylinders using pulsed HBr/O_2 plasma with (b) 120 s and (a, c) 200 s etching time.

layer is not entirely etched at the end of the silicon transfer etching process, a thin layer (25 nm) is still observed at the sample's surface after 200 s, protecting the upper part of the lines. The critical dimension (CD) of the lines is 15 ± 3 nm, which corresponds to both PDMS cylinder and SoC line dimensions produced in the earlier etching steps. This indicates that a good CD control is performed using this process.

It is important to underline that the CD control achieved in this process is due to the fact that the plasma is pulsed. Typical silicon etching processes in CW plasma fail to etch the silicon lines. The basic phenomena taking place during the two RF power phases can be explained as follows. During the ON phase, the plasma ignites and the electron (and ion) density rises to form H_2O^+, O_2^+, HBr^+, Br_2^+ reactive species.[30,21] The ions are accelerated to high energy (about 250 eV) by the self-

bias voltage that develops rapidly on the electrostatic chuck during this ON phase. Such a high energy allows the ions to reach the bottom of the trenches and assist in the etching process. Furthermore, the ion energy in pulsed plasma is high enough to sputter poorly volatile $SiBr_x$ species from the trench bottom. These species can redeposit on the feature sidewalls thus contributing importantly to their passivation.[31] In the ON period, electron dissociation reactions produce reactive radicals (O, Br, H, SiBrx) in the plasma which will stick on the sidewalls to form a protective $SiOBr_x$ passivation layer. However, it is well-known that due to shadowing effects, only the top of the high aspect ratio features can be protected by the passivation layer but not the bottom (oxygen atoms have a high sticking probability and cannot diffuse deep into the features).[32] The assistance of the SiBr species sputtered from the features bottom is expected to contribute significantly to form the sidewall passivation layers. The formed $Si_xO_yBr_z$ layers allow the anisotropic etching profiles as shown in Figure 5 b).

During the OFF phase, the inductive electric field, responsible for the electron heating, vanishes rapidly and the electron temperature cools down in 10 μs. Even though there is no production of radicals during this period, the radical density varies on time scales (several milliseconds) that are longer than the pulsing period (1 ms). Therefore, the radical density is only weakly modulated when the plasma is pulsed at 1 kHz or higher.[22] The plasma chemistry is controlled by the duty cycle (because radicals are produced in the ON period and lost in the OFF period) and the radical flux is the same in the OFF and ON periods. Hence, in the OFF period, radicals are participating to the passivation layer formation and enhance the Br coverage of the feature bottom. At the same time, the bias voltage drops rapidly to zero in the OFF period and the substrate is bombarded by very low energy ions. The low energy ions do not participate in the etching process but they are expected to be easily deflected by the negative charges accumulated on the mask and to neutralize them.

Pulsed plasma etching shows thus several benefits for high aspect ratio structure etching compared to continuous plasma etching. The particular chemical plasma composition, the bombardment of high energy ions in the ON period (which enhances etching and provides passivation) and low energy ions in the OFF period are expected to significantly improve the process.[33]

CONCLUSIONS AND PERSPECTIVES

We have generated periodic silicon line patterns by combining standard trilayer industry-type photolithography substrates with cylindrical high-χ BCP graphoepitaxy. Trenches realized in both the anti-reflective coating (SiARC) and the spin-on carbon (SoC) layers create guide lines for the directed self-assembly of the block copolymer. Horizontal cylinders were aligned within the trenches during solvent vapor annealing to form parallel features of PDMS in a PS matrix. Nanopatterns of oxidized PDMS were revealed by an HBr/O_2 plasma etch. Finally, the periodic patterns were transferred into the silicon substrate using dedicated pulsed plasma etching conditions. Silicon nanostructures with ~15 nm half-pitch line/space and a height up to 90 nm have been successfully obtained with a good control of the critical dimensions compared to the initial PDMS cylinder diameter. This process provides new opportunities for next-generation sub-10 nm lithography applications.

Further improvements and characterizations of the process are still ongoing. Concerning the SVA process, the work is dedicated to the decrease of the process time to a few minutes. First results show the importance of both the beginning and the end of the SVA process. A control of the swelling/deswelling rate in the annealing chamber would also be necessary to avoid the macroscopically observed dewetting defects. Controlling these defects is the key for an eventual integration of the PS-*b*-PDMS high-χ BCP into a microelectronics environment, and more generally onto large processing surfaces. On the other hand, more work is carried out on the measurement of the critical dimension uniformity (CDU) control during the whole etching process.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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Notes

The authors declare no competing financial interest.

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